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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,792	03/25/2004	Shunji Nakamura	040126	2791
23850	7590	08/04/2005	EXAMINER	
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP			NGUYEN, HA T	
1725 K STREET, NW			ART UNIT	
SUITE 1000			PAPER NUMBER	
WASHINGTON, DC 20006			2812	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/708,792	Applicant(s) NAKAMURA ET AL.	
	Examiner Ha T. Nguyen	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 1-5, 8, 10 and 17-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6, 9 and 14-16 is/are rejected.
- 7) ☒ Claim(s) 7 and 11-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3-25-4</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Notice to Applicants***

1a. Applicants' election of Species I, claims 6, 7, 9, and 11-16 in the response filed 7-16-5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 1038 and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 6, 9, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USPAPN 20050045947, hereinafter "Chen").

Referring to Figs. 4A-5B and corresponding text, Chen discloses [Re claim 6] a method of manufacturing a semiconductor device having a gate electrode formed on a semiconductor layer with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, comprising the steps of: forming a laminated region of a sacrificial layer 144, 146 and a semiconductor layer 150 and a device separating region 156 surrounding said

laminated region, on a substrate 142; forming a gate electrode 154 on said semiconductor layer with a gate insulating film 152 interposed therebetween; forming an opening 165 through which said sacrificial layer is exposed between said device separating region and said semiconductor layer; and removing said sacrificial layer through said opening to form a cavity below said semiconductor layer. But it fails to disclose expressly the electrode layer is also formed on said device separating region. However, the missing limitation is well known in the art because in the normal practice the device separating region (STI or field oxide) is formed before the formation of the gate electrode layer, in this case the gate electrode is deposited on exposed area including the device separating region. A person of ordinary skill is motivated to modify Chen to use a conventional practice of well known characteristics.

[Re claim 9] Chen discloses wherein said step of forming the laminated region and the device separating region comprises the steps of: forming said sacrificial layer and said semiconductor layer on said substrate to form said laminated region; and thereafter, forming said device separating region surrounding said laminated region and extending to said substrate (see par. [0028]-[0029]);

[Re claim 14] wherein said sacrificial layer comprises a BOX layer 144 of an SOI substrate, and said semiconductor layer comprises a thin-film semiconductor layer formed on an uppermost layer of said SOI substrate; and

[Re claim 15] before or after the step of removing said sacrificial layer, forming a source/drain in said semiconductor layer in sandwiching relation to a region directly below said gate electrode; and following said step of forming said source/drain (see Fig. 5A). It would have been obvious that silicidizing said source/drain entirely or partly to reduce resistivity of contact to the source/drain.

Therefore, it would have been obvious to use Chen's teaching to obtain the invention as specified in claims 6, 9, and 14-15.

3. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, as applied above, in view of Chidambarao et al.(USPN , hereinafter "Chidambarao").

Chen discloses substantially the limitations of claim 16, as shown above.

But it fails to disclose expressly forming another semiconductor layer on said semiconductor layer, and forming a source/drain in said semiconductor layer and said other semiconductor layer in sandwiching relation to a region directly below said gate electrode.

However, the missing limitation is well known in the art because Chidambarao discloses this feature (See Figs. 3-7, # 35,).

A person of ordinary skill is motivated to modify Chen with Chidambarao to obtain easy flow of carriers (see Chidambarao, col. 4, lines 10-16) .

Therefore, it would have been obvious to combine Chen with Chidambarao to obtain the invention as specified in claim 16.

Allowable Subject Matter

4. Claims 7 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 recites the step of "curving said semiconductor layer".

This feature in combination with the other elements of the claim is neither disclosed nor suggested by the prior art of record.

Claims 11-13 variously depend from claim 7, they are allowed for the same reason.

Conclusion

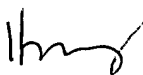
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ha Nguyen

Primary Examiner

8-1-05